



SHAPING THE NEXT GENERATION OF ELECTRONICS

**JUNE 23-27, 2024**

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# Fast and deterministic memory yield estimation using machine learning augmented statistical simulations

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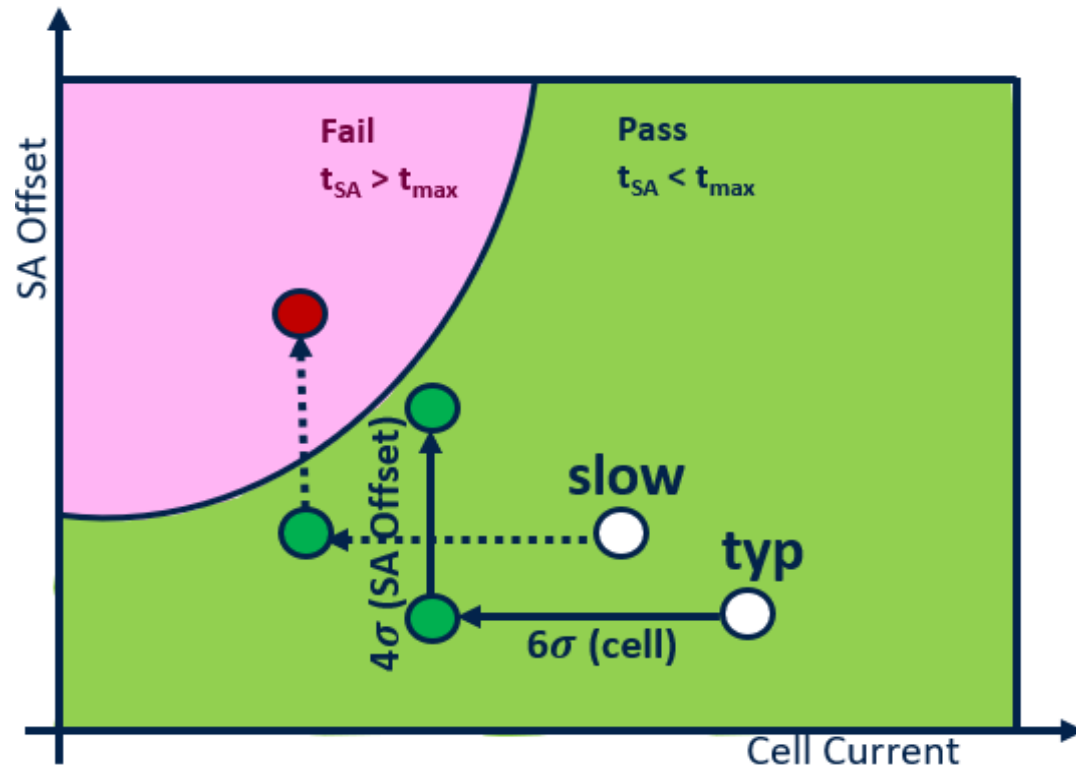
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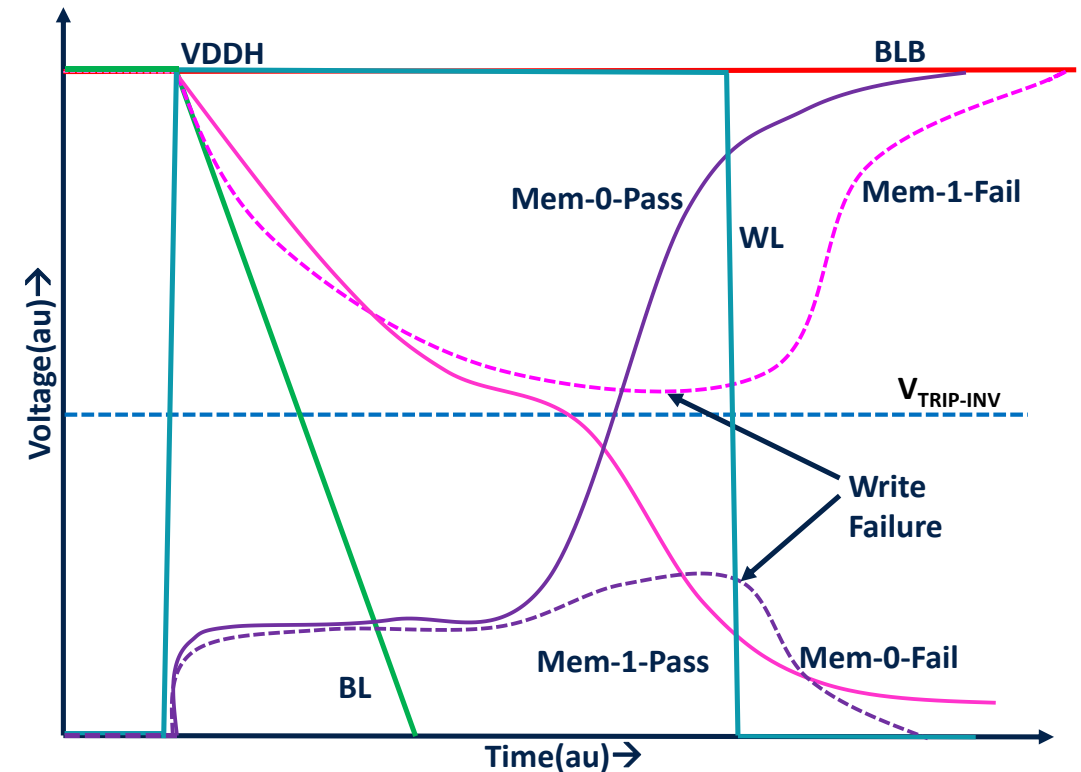




# DOMINANT FACTORS FOR MEMORY (SRAM) YIELD CONSIDERATIONS



Read failure probability in 6T-SRAM primarily depends on lcell and SA offset variations.

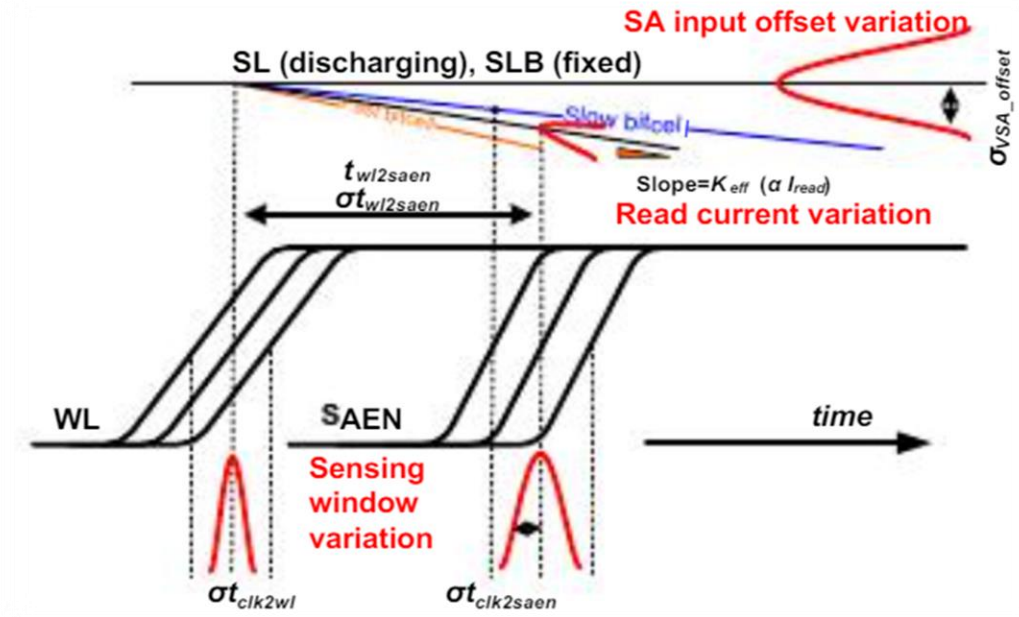
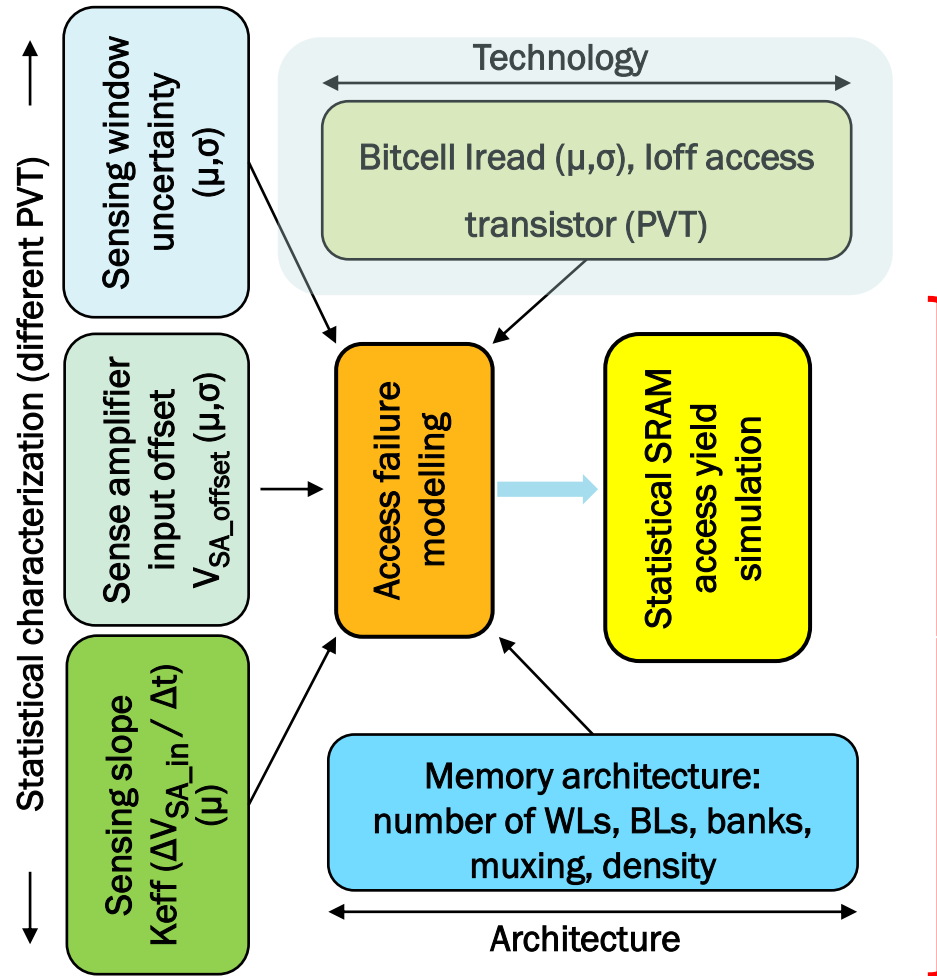


The wordline window should be adequate to avoid write failure due to statistical variations.

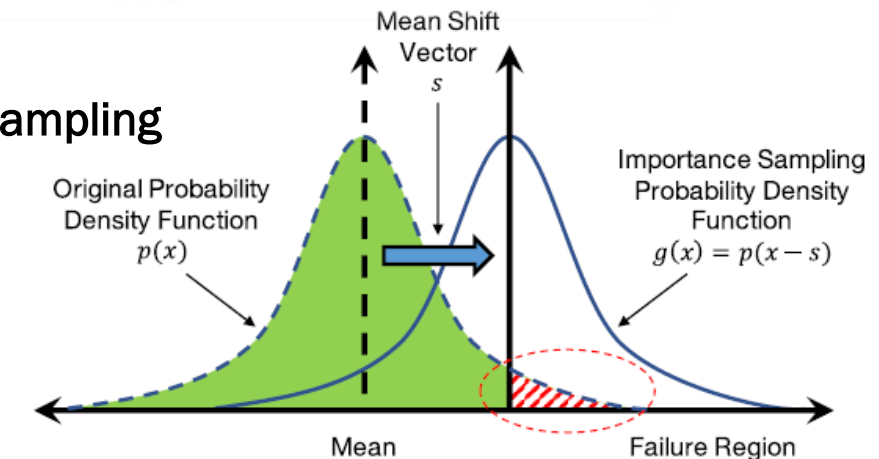
Statistical analysis at full-memory level is impractical using existing methods for very high sigma qualifications (>6)

# LIMITATIONS WITH EXISTING METHODOLOGIES

Limitations – Extremely large runtime and/or associated large inaccuracies



## Importance sampling

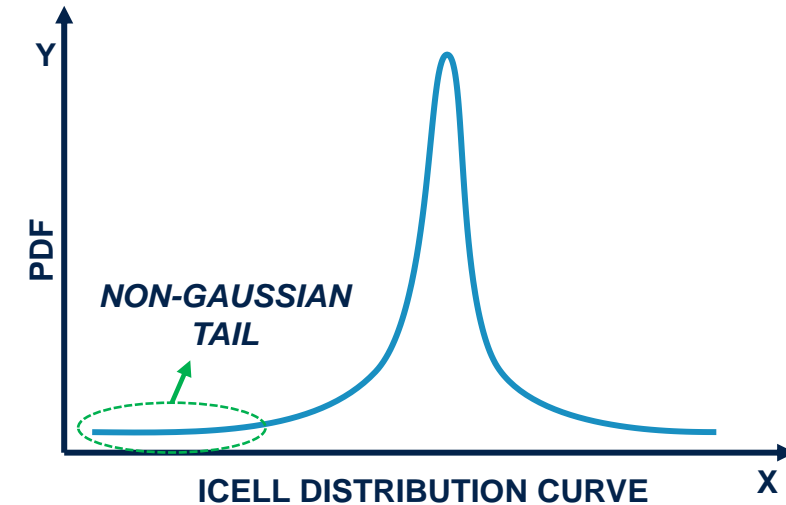


# LIMITATIONS WITH EXISTING METHODOLOGIES

Blocks	Counts (Repetition)	Sigma (99% yield)	No. of MC simulations
Bitcells	64 Mb	6.3	6.4 Billion

- Typical 64Mb SRAM usage on SoC requires  $\geq 6\sigma$  for bitcells
- This requires >6.4 billion samples to be simulated! Not feasible

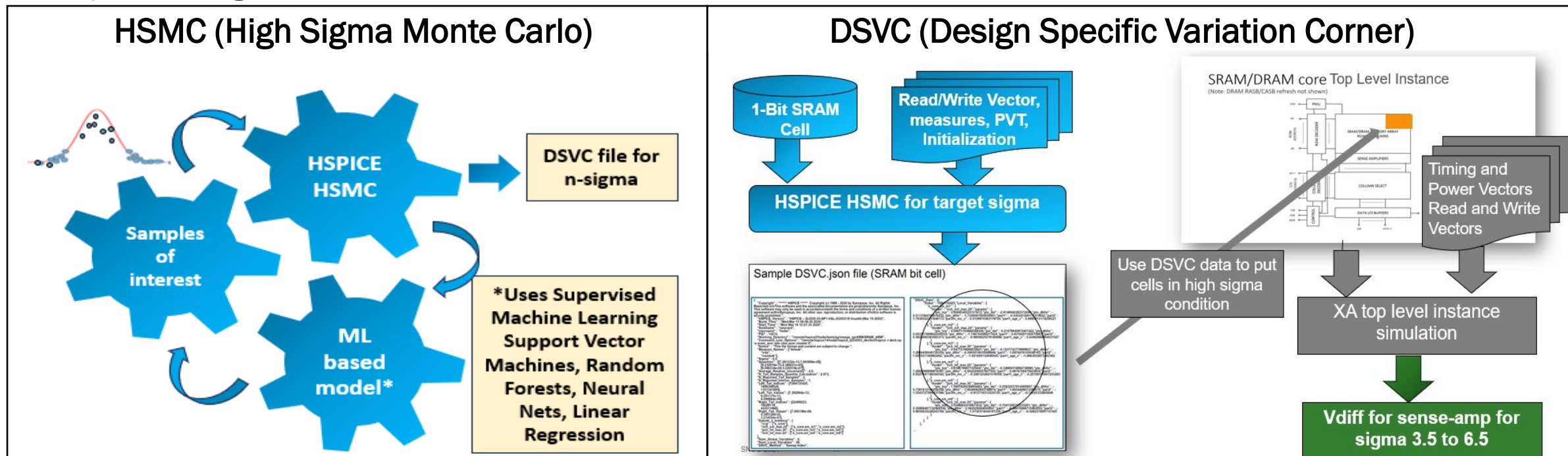
Bitcell current/ICELL ( $\mu\text{A}$ )	$-6\sigma$	$-5\sigma$	$-4\sigma$	$-3\sigma$	$3\sigma$	$4\sigma$	$5\sigma$	$6\sigma$
Real distribution (50M samples)	NA	3.36	4.50	5.95	20.35	23.70	27.7	NA
Estimated with Normal distribution (10K samples) $\mu = 12.02 / \sigma = 2.41$	-2.44	-0.04 (101%)	2.37 (47%)	4.78 (20%)	19.26 (5.3%)	21.67 (8.5%)	24.09 (13%)	26.48



- In a full-memory IP with  $6\sigma$  qualification target, 50 million samples can provide up to  $5\sigma$  ICELL
- Estimation assuming normal-distribution using 10K samples gives wrong results for ICELL
- Extended tail of ICELL distribution curve introduces inaccuracy with Gaussian approximation

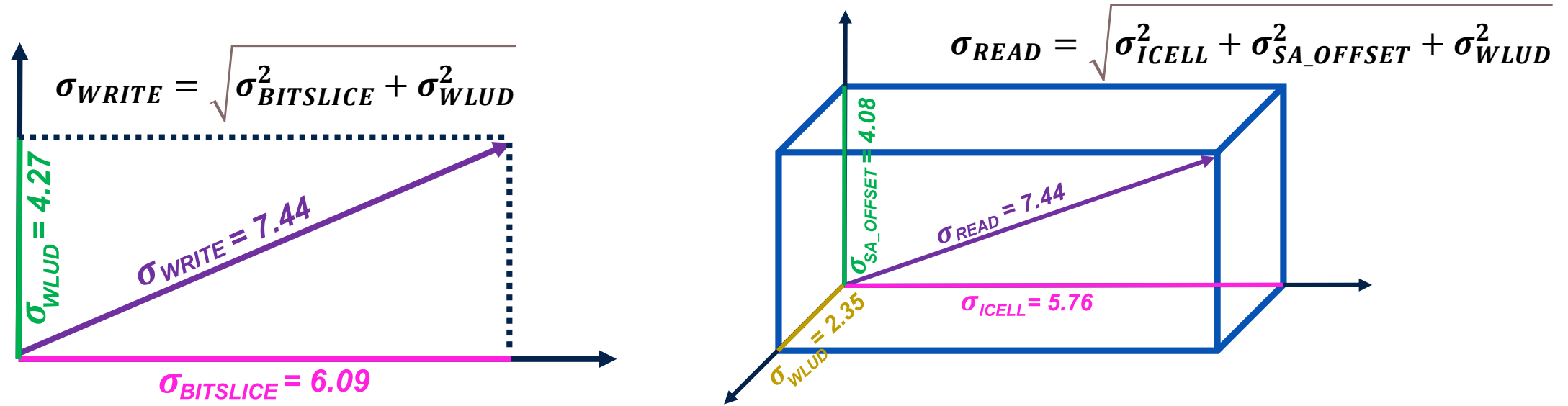
# EXTRACTING N-SIGMA PARAMETERS USING ML AUGMENTED STATISTICAL SIMULATIONS (HSMC+DSVC)

HSPICE and PrimeSim XA SPICE simulators from Synopsys are capable of high sigma statistical analysis using HSMC and DSVC features



- HSMC uses a surrogate model-based ML algorithm
- HSMC dumps n-sigma (e.g.,  $6.2\sigma$ ) representative spice model (**DSVC file**)
- DSVC file enables n-sigma representative simulation over full memory

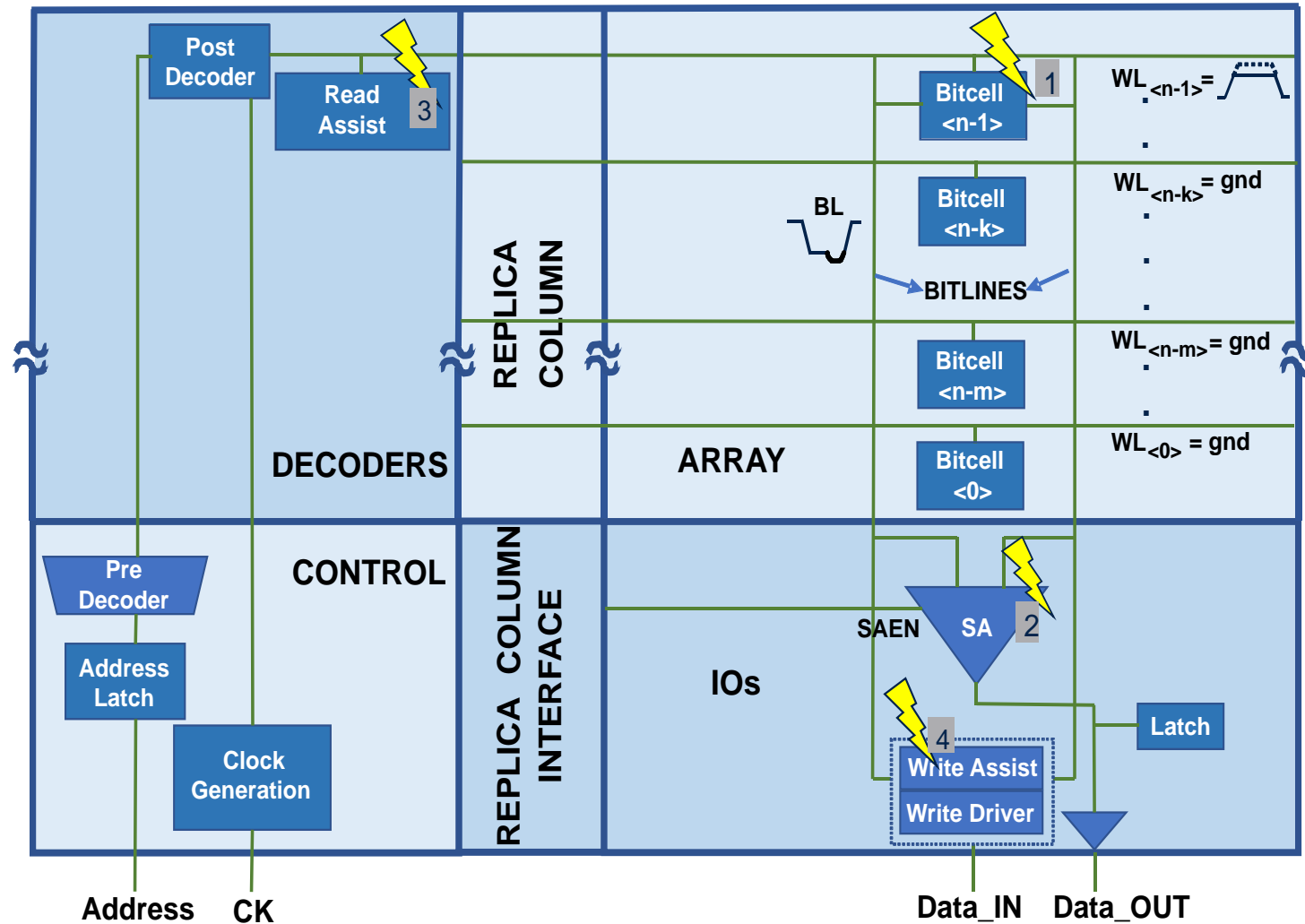
# MEMORY YIELD ESTIMATION USING HSMC+DSVC



- Target sigma ( $\sigma_{WRITE}$ ,  $\sigma_{READ}$ ) for memory yield estimation is defined by **target PPM** and **memory capacity on SoC**
- Dominant contributing factors for variations are **ICELL**, **WordLine-UnderDrive (WLUD)**, **BitSlice** and **sense amplifier** circuits
- Target sigma for contributing factors is derived by **sensitivity analysis**
- Sensitivity analysis is carried out by observing the **impact of  $1\sigma$  change** for respective circuits
  - E.g., impact of  $1\sigma$  change in ICELL towards VDIFF (differential voltage across bitlines)



# WRITE YIELD ESTIMATION USING HSMC+DSVC



Calculate target sigma for bitslice and WLUD

Get DSVC file for WLUD circuit using HSMC

Simulate full memory using DSVC file. Get interface signals for target write-bitslice

Evaluate sigma qualification of bitslice (~2k MOS) using HSMC

Write-assist level	$\sigma_{BITSlice}$	$\sigma_{WRITE}$
-256mV	6.46	7.74
-209mV	5.71	7.13
<b>-228mV</b>	<b>6.14</b>	<b>7.48</b>



# WRITE YIELD ESTIMATION USING HSMC+DSVC

- $3\sigma$  WLUD is determined using HSMC and used both in READ and WRITE yield estimation
- (TYPICAL +  $3\sigma$ ) WLUD is utilized for stability purpose
- (TYPICAL -  $3\sigma$ ) WLUD is utilized for self-time purpose

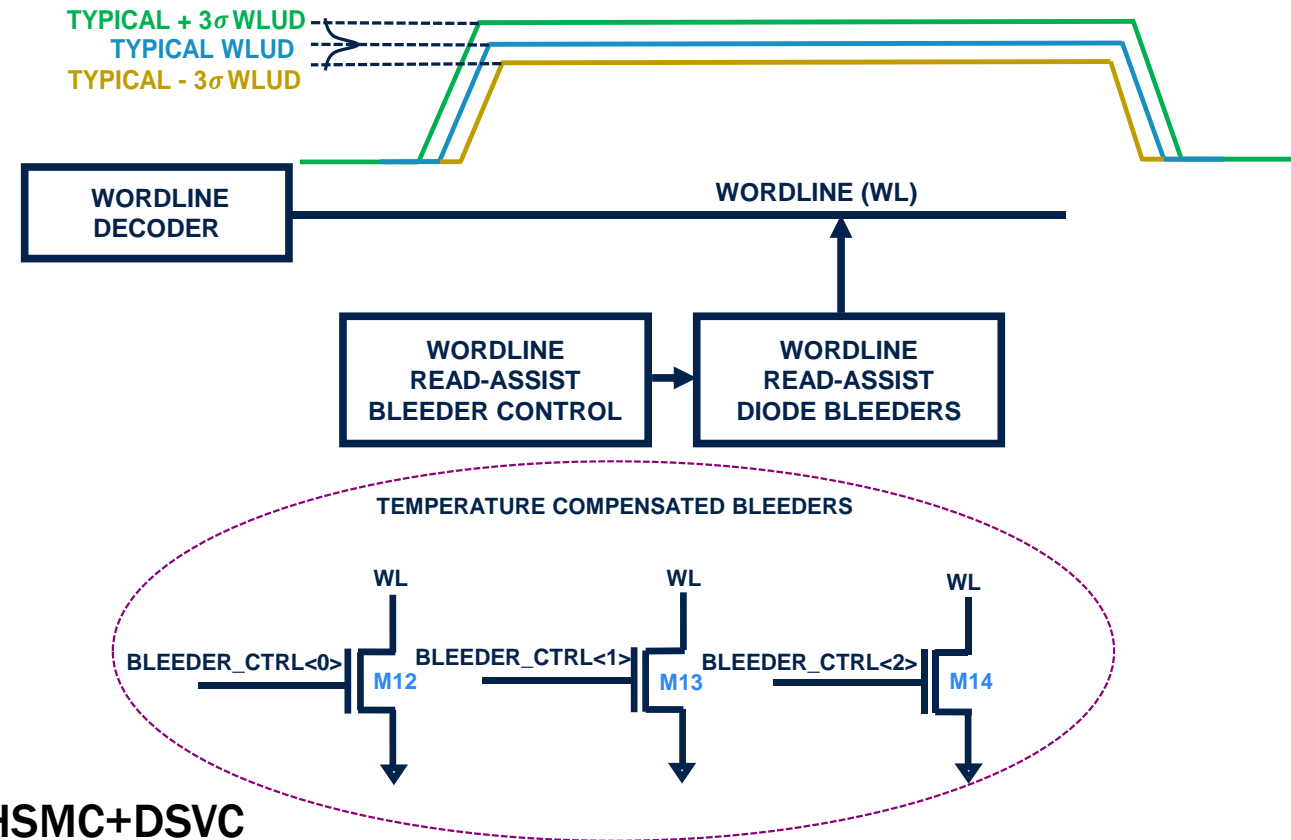
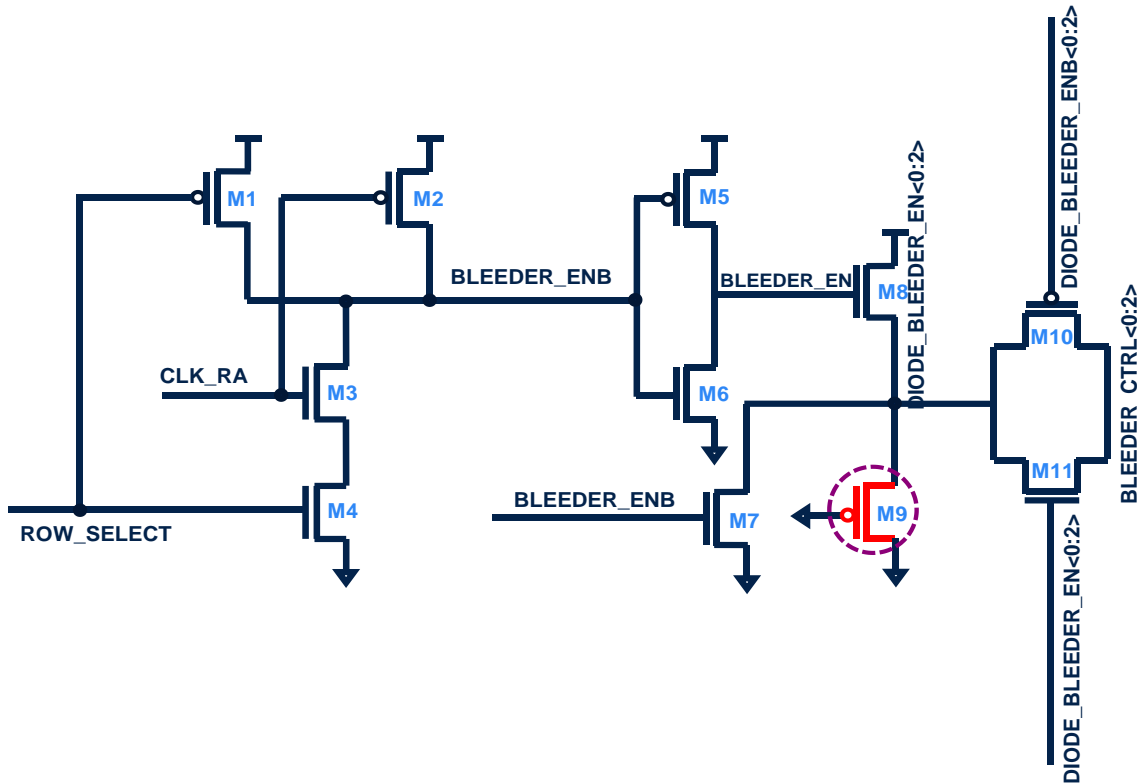


Illustration of n-sigma WLUD estimation by HSMC+DSVC

# WRITE YIELD ESTIMATION USING HSMC+DSVC

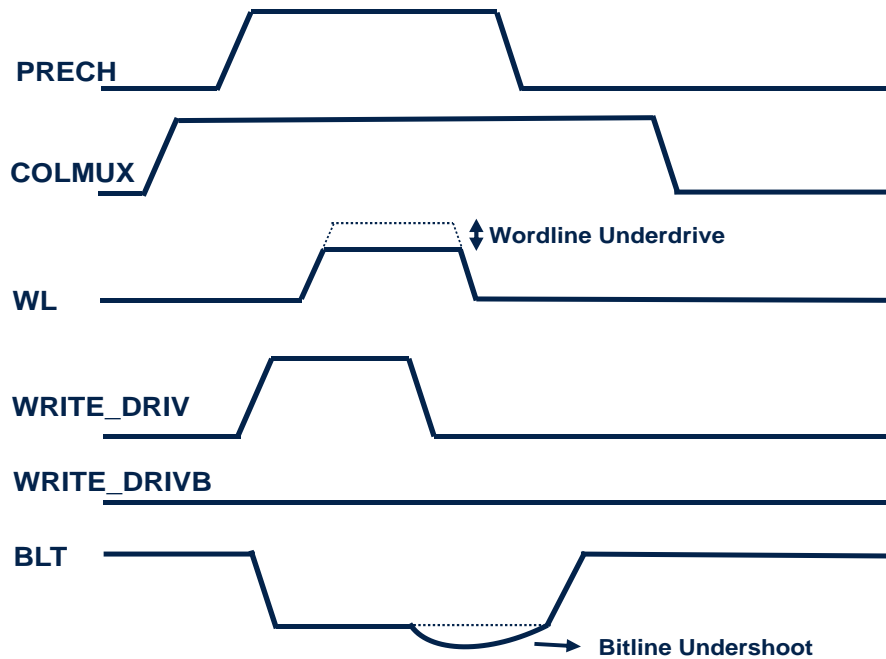
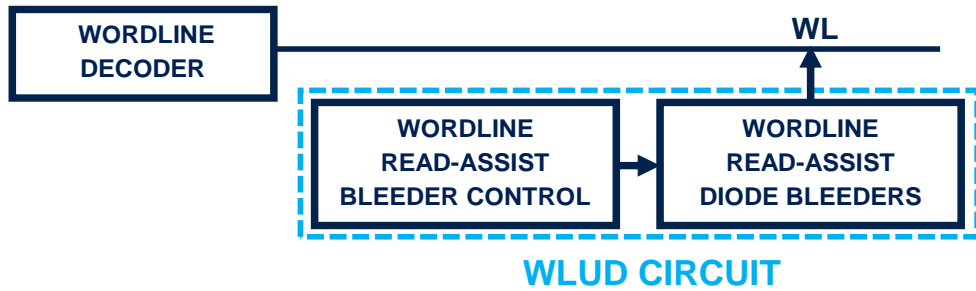
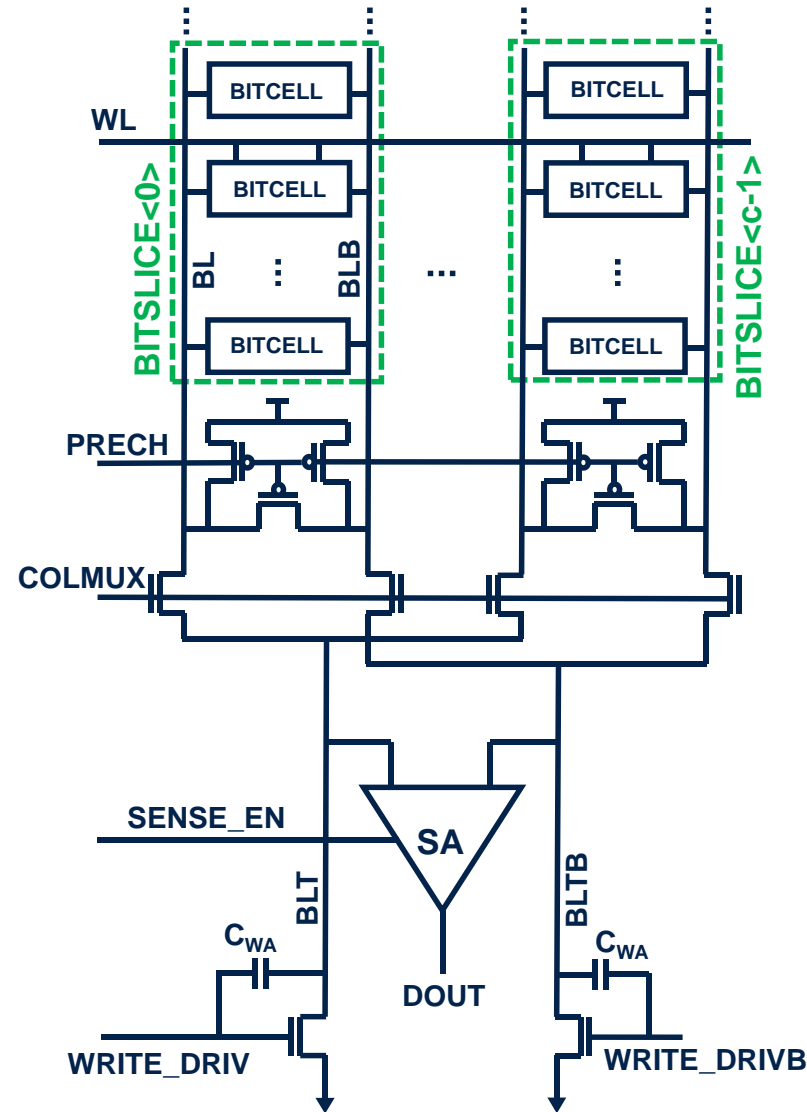


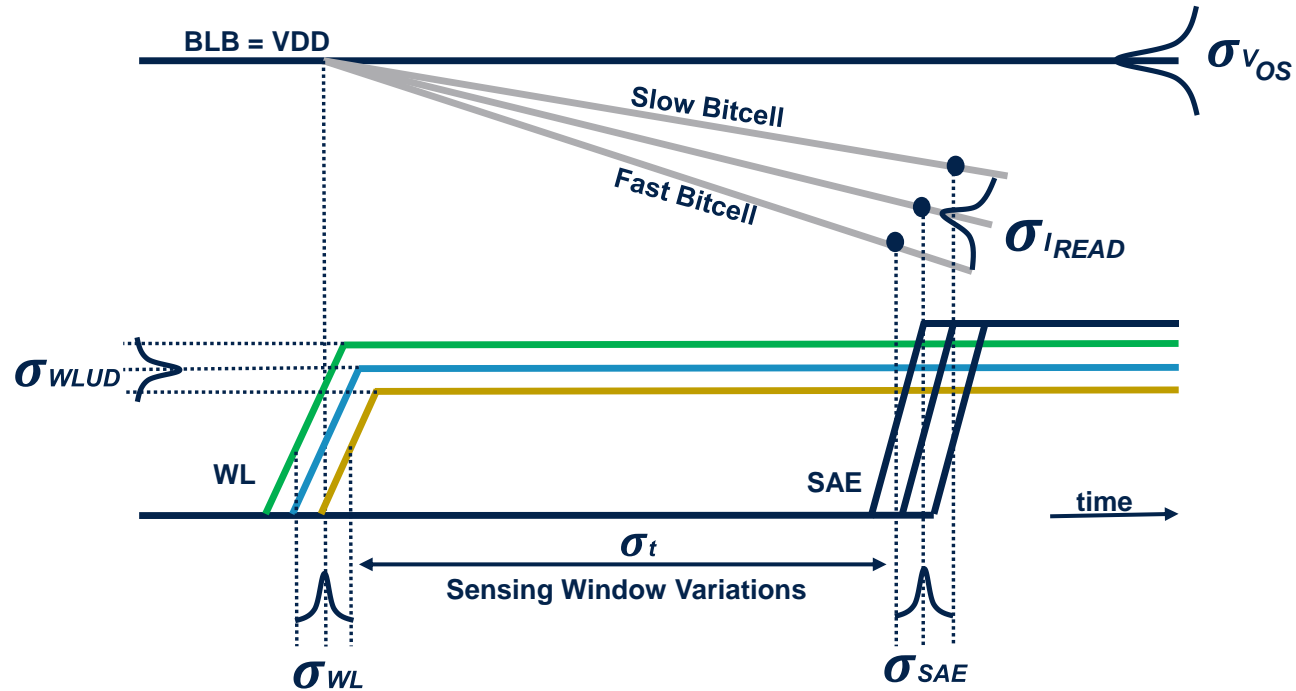
Illustration of simplified block arrangement during write operation



True interfacing signals are captured for bitslice in a nominal simulation

HSMC is used for precise determination of n-sigma write qualification of bitslice (~2000 devices)

# READ YIELD ESTIMATION USING HSMC+DSVC



SAE: sense amplifier enable  
WL: wordline

Calculate target sigma for bitcell, SA and WLUD

Get DSVC file for above circuits using HSMC

Simulate full memory using DSVC file

Adjust replica path for correct READ operation with minimum delay

Replica delay	READ status
1.20 ns	PASS
1.10 ns	FAIL
1.16 ns	FAIL
1.18 ns	PASS

# RESULTS

- Memory yield analysis is performed for a high-density single port SRAM in 40 nm CMOS technology supporting functional  $V_{min}$  of 0.81 V, considering a capacity of **64 Mbytes** and **10 PPM** target
- We could ensure a WRITE sigma qualification of **7.48** and READ sigma qualification of **7.44**



# CONCLUSIONS

- Yield estimation of **64 Mbytes** SRAM with Brute-force Monte Carlo is impractical due to **>1 billion** samples
- Importance sampling is fast but inaccurate
- Memory yield estimation is evaluated using **HSMC & DSVC** technologies by Synopsys
- The proposed methodology is more accurate and faster due to the ML algorithm
- The proposed methodology reduces memory yield estimation time from **~2 weeks to ~1 day**



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# THANK YOU!





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# QUESTIONS !

